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EXAMINER

MOE, AUNG SOE

ART UNIT	PAPER NUMBER
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2612

DATE MAILED: 05/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/965,095

Applicant(s)

ONUKE, MASAO

Examiner

Aung S. Moe

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 March 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) 16-21 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 08/900,446.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>9/28/2001</u> . | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

Election/Restriction

1. Applicant's election with traverse of Group (I), Claims 1-15 in Paper No. 6 is acknowledged. The traversal is on the ground(s) that the subject matter of all claims (1-21) is sufficiently related that a through search for the subject matter of any one Group of claims would necessarily encompass a search for the subject matter of the remaining claims. This is not found persuasive because according to MPEP section 803, a serious burden on the Examiner may be *prima facie* shown if the Examiner shows by appropriate explanation either separate classifications, separate status in the art, or a different field of searches.

In this case, the Examiner clearly set forth in the last Office Action that the search for the invention I (claims 1-15) does not require a search for the invention II (claims 15-21). Moreover, it is further noted that the invention I and II are distinct from each other because the invention I is mutually exclusive from the invention II.

In view of this, the mere evidence of the patentably distinct inventions, separate status in the art (i.e., noted that Group I is classified in class 348/231 and Group II is classified in 348/207), and the different fields of searches are *prima facie* evidence of examining burdens of the Examiner.

The requirement is still deemed proper and is therefore made **FINAL**.

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2. Claims 16-21 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention (Group II, claims 16-21), there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper No. 6.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

5. Claims 3-5, 7-9, and 10-13 are objected to because of the following informalities:

In claim 3, it is unclear how Aexternal devices≡ as recited in line 4 relates to Aexternal devices≡ as recited in claim 1, line 9? If there are the same Aexternal devices≡, the Examiner suggests changing Aexternal devices≡ in claim 3, lines 4 to --said external devices--.

As for claim 4, it is noted that claim 4 dependent on the rejected-based claim 3 and therefore inherits the deficiencies thereof.

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In claim 5, it is unclear how Aexternal devices≡ as recited in line 2 relates to Aexternal devices≡ as recited in claim 1, line 9? If there is the same Aexternal devices≡, the Examiner suggests changing Aexternal devices≡ in claim 5, lines 2 to --said external devices--.

In claim 7, please change Athe device≡ as recited in lines 1 & 2 to --the information processing device--.

In claim 7, please change Athe object≡ as recited in line 4 to --an object--.

As for claim 8, it is noted that claim 8 dependent on the rejected-based claim 7 and therefore inherits the deficiencies thereof.

In claim 9, it is unclear how Aexternal devices≡ as recited in line 2 relates to Aexternal devices≡ as recited in claim 6, line 8? If there is the same Aexternal devices≡, the Examiner suggests changing Aexternal devices≡ in claim 9, lines 2 to --said external devices--.

In claim 10, it is unclear how Aan external device≡ as recited in lines 9+ relates to Aan external device≡ as recited in claim 10, line 5? If there is the same Aexternal device≡, the Examiner suggests changing Aan external device≡ in claim 10, lines 9-10 to --said external device--.

In claim 11, please change Athe device≡ as recited in line 1 to --the information processing device--.

In claim 11, please change Athe object≡ as recited in line 3 to --an object--.

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In claim 12, it is unclear how Aan external device≡ as recited in line 6 relates to Aan external device≡ as recited in claim 10, line 5? If there is the same Aexternal device≡, the Examiner suggests changing Aan external device≡ in claim 12, lines 6 to --said external device--.

In claim 13, it is unclear how Aan external device≡ as recited in line 4 relates to Aan external device≡ as recited in claim 10, line 5? If there is the same Aexternal device≡, the Examiner suggests changing Aan external device≡ in claim 13, lines 4 to --said external device--.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 5-6, 9-10 and 13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamauchi (U.S. 5,097,445).

Regarding claim 1, Yamauchi >445 discloses an information processing device (i.e., Fig. 1, the semiconductor integrated circuit A) comprising:

storage means (i.e., Fig. 1, the element 41) for storing data, said storage means having a first region (i.e., Fig. 4, the element 41c/41d) and second region (Fig. 4, the element 41b), both of which are capable of storing data (col. 5, lines 60-68);

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connection means (Fig. 1, the elements 5a, 5b; col. 3, lines 45-50) for enabling the information processing device (A) to be connected to an external device (i.e., the External reader/writer or the CPU 1; col. 4, lines 65+) that is separate from the information processing device (A); and

prevention means (i.e., the inhibiting means 58 as shown in Fig. 1) for preventing external devices (i.e., the External reader/writer and the CPU 1) connected to the connection means (i.e., 5a/5b) for accessing the first region (i.e., inhibiting the reading/writing of data from the inhibiting area 41c/41d; see col. 2, lines 60+, col. 6, lines 1-15 and col. 6, lines 30-36).

Regarding claim 5, Yamauchi >445 discloses wherein the prevention means (i.e., the element 58 of Fig. 1) enables the external devices connected to the connection means to access the second region (41b) of the storage means (i.e., col. 6, lines 37-41).

Regarding claim 6, Yamauchi >445 discloses an information processing device (i.e., Fig. 1, the semiconductor integrated circuit A) comprising:

a memory (i.e., Fig. 1, the element 41) having a first storage region (i.e., Fig. 4, the element 41c/41d) and a second storage region (Fig. 4, the element 41b);

a connector (Fig. 1, the elements 5a, 5b) by which the information processing device can be connected to an external device (i.e., the External reader/writer or the CPU 1; col. 4, lines 65+) that is separate from the information processing device (A); and

a controller (i.e., the inhibiting control circuit 58 as shown in Fig. 1) coupled to the connector and to the memory, the controller preventing (i.e., inhibiting) the external devices

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(i.e., the External reader/writer and the CPU 1) connected to the connector (5a/5b) from accessing the first storage region (41c/41d) of the memory (i.e., inhibiting the reading/writing of data from the inhibiting area 41c/41d; see col. 2, lines 60+, col. 6, lines 1-15 and col. 6, lines 30-36).

Regarding claim 9, Yamauchi >445 discloses wherein the controller (i.e., the inhibiting control circuit 58 as shown in Fig. 1) enables external devices connected to the connection means to access the second region of the memory (i.e., col. 6, lines 37-41).

Regarding claim 10, Yamauchi >445 discloses a method of controlling an information processing device (i.e., Fig. 1, the semiconductor integrated circuit A) having a memory (41) that is partitioned into a first storage region (i.e., Fig. 4, the element 41c/41d) and a second storage region (Fig. 4, the element 41b), and a connector (Fig. 1, the elements 5a, 5b) by which the information processing device (A) can be connected to an external device (i.e., the External reader/writer or the CPU 1; col. 4, lines 65+) that is separate from the information processing device (A); the method comprising the steps of:

determining whether a request to access the first storage region (i.e., 41c/41d of the memory 41) of the memory is initiated by an external device (i.e., the External reader/writer or the CPU 1) connected to the connector (col. 5, lines 5+; Figs. 3a-3b); and

denying (i.e., inhibiting) access to the first storage region of the memory if the request was initiated by the external device (i.e., col. 2, lines 61+, col. 6, lines 34-36; Figs. 3a-3b).

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Regarding claim 13, Yamauchi >445 further discloses the step of enabling external devices connected to the connected to the connector to access the second region of the memory (i.e., the region 41b of the memory 41 as shown in Fig. 4) when the external device connected (i.e., the External reader/writer or the CPU 1) to the connector requests access to the second storage region of the memory (i.e., col. 6, lines 37-41).

Regarding claim 14, Yamauchi >445 discloses wherein the request to access is a request to write data to the first storage region of the memory (i.e., see col. 5, lines 20+ and col. 5, lines 38-41).

Regarding claim 15, Yamauchi >445 discloses wherein the request to access is a request to red data from the first storage region of the memory (i.e., see col. 5, lines 55+).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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9. Claims 1-4 and 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki et al. (U.S. 5,867,218) in view of Yamauchi (U.S. 5,097,445).

Regarding claim 1, Matsuzaki >218 discloses an information processing device (i.e., Figs. 1 and 3) comprising:

storage means (i.e., a semiconductor memory 17; see col. 1, line 32 and col. 3, line 58) for storing data, said storage means capable of storing data (i.e., the image data stored in the semiconductor memory 17; see col. 4, line 25 and col. 5, lines 5+);

connection means (Figs. 1 & 3, the elements 14, 16f and 16e; see col. 5, lines 13-25) for enabling the information processing device (1) to be connected to an external device (i.e., the information unit/terminal 3, such as a personal computer, PDA and electronic notes; see col. 1, lines 10-15) that is separate from the information processing device (1).

Furthermore, although Matsuzaki >218 shows that the connection means (14/16f/16e) is capable of accessing the storage means (i.e., the image data recorded area of the memory 17b) for sending out signals to external devices (i.e., col. 2, lines 64) when the information processing device (1) is connected to external devices (i.e., the information unit/terminal 3; col. 1, lines 10+), Matsuzaki >218 does not explicitly show the use of storage means having a first region and a second region, both of which are capable of storing data and prevention means for preventing external devices from accessing the first region of the storage means as required by the present claimed invention.

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However, the above-mentioned claimed limitations are well-known in the art as evidenced by Yamauchi >445. In particular, Yamauchi >445 teaches the use of a semiconductor storage device (i.e., the element 41) having a first region (i.e., the protected data region as shown in Fig. 4) and second region (i.e., 41b as shown in Fig. 4), both of which are capable of storing data (i.e., see Fig. 4) and connecting means (i.e., Fig. 1, the elements 5a/5b) for enabling the information processing device to be connected to the external device (i.e., an external computer CPU 1 as shown in Fig. 1) that is separate from the information processing device (A); and prevention means (i.e., the inhibiting means 58 as shown in Fig. 1) for preventing the external device (i.e., an external computer CPU 1 as shown in Fig. 1) from accessing the first region of the storage means (i.e., the protected data region 41c/41d of the memory 41 as shown in Fig. 4) as required by the present claimed invention so as to prevent an important data file (i.e., the user=s secrete code) from being erroneously re-write or access by the external device (i.e., col. 2, lines 50+, and col. 6, lines 34+ of Yamauchi >445).

In view of this, having the system of Matsuzaki >218 and then given the well-established teaching of Yamauchi >445, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Matsuzaki >218 by providing the memory means and preventing means as taught by Yamauchi >445, since Yamauchi >445 states at col. 2, lines 52+ that such a modification would prevent erroneous re-writing of a program or an important data (i.e., the user=s secret code) stored in the memory device and thus, improved reliability and confidential property thereof. Moreover, such advantages as taught by Yamauchi

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>445 are obviously desirable because when the camera system of Matsuzaki >218 is connected to the external devices (i.e., a personal computer, PDA and electronic notes; see col. 1, lines 10+ of Matsuzaki >218), erroneous rewriting of a program or protection-required data stored in the first region of the memory of the camera may be prevented as suggested by Yamauchi >445.

Regarding claim 2, Matsuzaki >218 discloses that the device further comprising: photography means (i.e., the element 11 as shown in Fig. 1 of Matsuzaki >218), located in the information processing device (1), for photographing an object (i.e., the element 4 as shown in Fig.2) and generating electronic image data of the object (col. 4, line 20+ of Matsuzaki >218); and processing means (i.e., Fig. 3, the element 16a), located in the information processing device (1), for processing the electronic image data.

Regarding claim 3, Matsuzaki >218 discloses wherein the electronic image data generated by the photography means (i.e., Fig. 3, the element 11) is stored in the storage means (i.e., noted the use of memory 17 as shown in Fig. 3), and Yamauchi >445 teaches the use of the prevention means (i.e., the circuit 58 as taught by Yamauchi >445) enables the external devices (i.e., the information unit/terminal 3; col. 1, lines 10+ of Matsuzaki >218) connected to the connection means (i.e., the element 14/16f as shown by Matsuzaki >218) to access the storage means (i.e., the region where the image data are stored in the memory 17). Although Matsuzaki >218 not specifically specifying the particular region of memory (17) for storing the image data from the photoelectric converter (11b), the memory used in the system of Matsuzaki >218 is

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extremely well-known in the art to pertain a different storage region for separately storing the image data and the image related data such as the Header data, ID data and the Management data so as to permit external devices (i.e., the information unit/terminal 3, such as a personal computer), via I/F 16f, to readily recognize and access the data stored on the memory (17). This is further evidenced by the memory (14) of Yamauchi >445.

Furthermore, Yamauchi >445 teaches that the preventing means (i.e., the circuit 58 of Yamauchi >445) enables the external devices (i.e., Fig. 1, the External Reader/Writer or CPU as taught by Yamauchi >445) connected to the connection means (i.e., the element 14/16f as shown by Matsuzaki >218) to access the second region of the storage means (i.e., the region 41b of the memory 41 as taught by Yamauchi >445; see col. 6, lines 38).

In view of this, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the prevention means as taught by Yamauchi >445 to allow the external devices to access the second region of the memory where unprotected image data may be readout to the external devices, i.e., such as a computer, so that the memory of the camera will always have the necessary capacity to preserve all of the images desired to be captured by the camera, thus, it is possible to perform photography without any limitation being imposed on the number of images that can be shot by the camera of Matsuzaki >218.

Regarding claim 4, the combination of Matsuzaki >218 and Yamauchi >445 discloses wherein the photography means (i.e., the element 11 of Matsuzaki >218) includes a lens (11a)

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and a photoelectric converter (11b) upon which the lens focuses an image of the object so that the photoelectric converter generates the electronic image data (i.e., col. 4, lines 32+ of Matsuzaki >218), such that the information processing device is an electronic camera (i.e., the element 1 as shown in Fig. 2 of Matsuzaki >218 is an electronic camera; col. 1, lines 31+ of Matsuzaki >218).

Regarding claim 6, Matsuzaki >218 discloses an information processing device (i.e., Figs. 1 and 3) comprising: a memory (i.e., a semiconductor memory 17; see col. 1, line 32 and col. 3, line 58);

a connector (i.e., Figs. 1 & 3, the elements 14, 16f and 16e; see col. 5, lines 13-25) by which the information processing device (1) can be connected to an external device that is separate from the information processing device (i.e., the information unit/terminal 3, such as a personal computer, PDA and electronic notes; see col. 1, lines 10-15); and

a controller (i.e., see Fig. 1, the elements 16c/16e) coupled to the connector (i.e., see Fig. 1, the element 16f) and to the memory (17a/17b).

Furthermore, although Matsuzaki >218 shows that the connector (14/16f/16e) is capable of accessing the memory (i.e., the image data recorded area of the memory 17b) for sending out signals to external devices (i.e., col. 2, lines 64) when the information processing device (1) is connected to external devices (i.e., the information unit/terminal 3; col. 1, lines 10+), Matsuzaki >218 does not explicitly show the use of a memory having a first region and a second region, and

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the controller preventing the external devices connected to the connector from accessing the first storage region of the memory as required by the present claimed invention.

However, the above-mentioned claimed limitations are well-known in the art as evidenced by Yamauchi >445. In particular, Yamauchi >445 teaches the use of a semiconductor storage device (i.e., the element 41) having a first region (i.e., the protected data region as shown in Fig. 4) and second region (i.e., 41b; see Fig. 4), and a connector (i.e., Fig. 1, the elements 5a/5b) by which the information processing device can be connected to the external device (i.e., an external computer CPU 1 as shown in Fig. 1) that is separate from the information processing device (A); and controller (i.e., the inhibiting means 58 as shown in Fig. 1) for preventing the external device (i.e., an external computer CPU 1 as shown in Fig. 1) from accessing the first region of the storage means (i.e., the protected region of the memory 41 as shown in Fig. 4) as required by the present claimed invention so as to prevent an important data file (i.e., the user=s secrete code) from being erroneously re-write or access by the external device (i.e., col. 2, lines 50+, and col. 6, lines 34+ of Yamauchi >445).

In view of this, having the system of Matsuzaki >218 and then given the well-established teaching of Yamauchi >445, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Matsuzaki >218 by providing the memory means and preventing means as taught by Yamauchi >445, since Yamauchi >445 states at col. 2, lines 52+ that such a modification would prevent erroneous re-writing of a program or an important data (i.e., the user=s secret code) stored in the memory device and thus, improved

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reliability and confidential property thereof. Moreover, such advantages as taught by Yamauchi >445 are obviously desirable because when the camera system of Matsuzaki >218 is connected to the external devices (i.e., a personal computer, PDA and electronic notes; see col. 1, lines 10+ of Matsuzaki >218), erroneous rewriting of a program or protection-required data stored in the first region of the memory of the camera may be prevented as suggested by Yamauchi >445.

Regarding claim 7, Matsuzaki >218 discloses wherein the device is an electronic camera (i.e., the element 1 as shown in Fig. 2 of Matsuzaki >218 is an electronic camera; col. 1, lines 31+ of Matsuzaki >218), the device further comprising:

a lens (11a), and a photoelectric converter (11b) upon which the lens focuses an image of the object so that the photoelectric converter generates electronic image data (col. 4, lines 32+), the lens (11a) and the photoelectric converter (11b) located in a housing of the electronic camera (1) (see Fig. 3); wherein: the controller (16c) is coupled to the photoelectric converter (11b) and controls the storage of the electronic image data in the memory (17) (see Fig. 3, col. 4, lines 51+).

Regarding claim 8, Matsuzaki >218 discloses wherein the controller (16c) stores the electronic image data generated by the photoelectric converter (11b) in the memory (17), and the controller (16c) enables external devices (i.e., the information unit/terminal 3) connected to the connector (16f) to access the memory (17)(col. 5, lines 10+), and Yamauchi >445 teaches the use of the controller (i.e., the circuit 58 as taught by Yamauchi >445) enables the external devices

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(i.e., the information unit/terminal 3; col. 1, lines 10+ of Matsuzaki >218 and Fig. 1, the External Reader/Writer or CPU as taught by Yamauchi >445) connected to the connection means (i.e., the element 14/16f as shown by Matsuzaki >218) to access the second region of the storage means (i.e., the region 41b of the memory 41 as taught by Yamauchi >445; see col. 6, lines 38).

Although Matsuzaki >218 not specifically specifying the particular region of memory (17) for storing the image data form the photoelectric converter (11b), the memory used in the system of Matsuzaki >218 is extremely well-known in the art to pertain a different storage region for separately storing the image data and the image related data such as the Header data, ID data and the Management data so as to permit external devices (i.e., the information unit/terminal 3, such as a personal computer), via I/F 16f, to readily recognize and access the data stored on the memory (17). This is further evidenced by the memory (14) of Yamauchi >445.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize Acontroller≡ as taught by Yamauchi >445 to allow the external devices to access the second region of the memory where unprotected image data may be readout to the external devices, i.e., such as a computer, so that the memory of the camera will always have the necessary capacity to preserve all of the images desired to be captured by the camera, thus, it is possible to perform photography without any limitation being imposed on the number of images that can be shot by the camera of Matsuzaki >218.

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10. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (U.S. 6,031,964) in view of Yamauchi (U.S. 5,097,445).

Regarding claim 10, Anderson >964 discloses a method of controlling an information processing device (Fig. 1, the element 110) having a memory (Fig. 5, col. 2, lines 18-20) and a connector (i.e., the elements 348) by which the information processing device (110) can be connected to an external device (i.e., an external host computer; see col. 3, lines 5-7) that is separate from the information processing device (110); the method comprising the steps of:

determining whether a request to access the first storage region of the memory is initiated by an external device connected to the connector (i.e., noted that Anderson >964 stated at col. 5, lines 35 that the memory, e.g., RAM disk 532, is organized in a Asectored \cong format similar to that of conventional hard disk drives, thus, it is cleared that the memory 532 may contain more than one storage region; also see col. 8, lines 6-7); and denying access to the storage region of the memory (col. 8, lines 7-8 and Fig. 11).

Moreover, it is noted that Anderson >964 stated at col. 5, lines 35 that the memory, e.g., RAM disk 532, is organized in a Asectored \cong format (i.e., noted the Asectored \cong format of ROM as shown in Fig. 5) similar to that of conventional hard disk drives, thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to partition the memory 532 into different sectors/regions such as a first storage region and a second storage region, since it was known in the art that by storing the image data file such as a second storage region of the memory and storing Address data in the first storage region of the memory, it

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would allow the external host computer to readily recognize and access the data stored on the camera's memory as suggested by Anderson >946 (col. 5, lines 35+ of Anderson >946).

Furthermore, although Anderson >964 shows the step of denying access to the storage region as shown in Fig. 11, Anderson >964 does not explicitly shows the steps of denying access to the first storage region of the memory.

However, the above-mentioned claimed limitations are well-known in the art as evidenced by Yamauchi >445. In particular, Yamauchi >445 teaches the use of a memory that is partitioned into a first storage region (i.e., 14b as shown in Fig. 4) and second storage region (i.e., the protected data region as shown in Fig. 4) and the step of denying access to the first storage region of the memory if the request was initiated by the external device(i.e., col. 2, lines 61+, col. 6, lines 34-36; Figs. 3a-3b) so as to prevent an important data file (i.e., the user's secret code) from being erroneously re-write or access by the external device (i.e., col. 2, lines 50+, and col. 6, lines 34+ of Yamauchi >445).

In view of this, having the method of controlling an information processing device (110) as discloses by Anderson >946 and then given the well-established teaching of Yamauchi >445, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Anderson >946 as taught by Yamauchi >445, since Yamauchi >445 states at col. 2, lines 52+ that such a modification would prevent erroneous re-writing of a program or an important data (i.e., the user's secret code) stored in the memory device and thus,

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improved reliability and confidential property thereof. Moreover, such advantages as taught by Yamauchi >445 are obviously desirable because when the camera system of Matsuzaki >218 is connected to the external device (i.e., a host computer; see col. 5, lines 35+ of Anderson >946), erroneous rewriting of a program or protection-required data stored in the first region of the memory of the camera may be prevented as suggested by Yamauchi >445.

Regarding claim 11, Anderson >946 discloses wherein the device is an electronic camera (col. 3, lines 9+) having a lens (220) and a photoelectric converter (224) upon which the lens focuses an image of an object (112) so that the photoelectric converter generates electronic image data (col. 3, lines 12-15), the lens (220) and the photoelectric converter (224) located in a housing of the electronic camera (110); wherein the electronic image data is stored in the memory (col. 5, lines 32+).

Regarding claim 12, Anderson >946 discloses that the electronic image data generated by the photoelectric converter (224) is stored in the memory (i.e., DRAM 346/RAM 532) and enabling the external device to access the image data storage region of the memory.

Yamauchi >445 teaches the step of enabling external devices (i.e., the External Reader/Writer or the External CPU as shown in Fig 1 of Yamauchi >445) connected to the connector to access the second region of the memory (41b) when the external device connected to the connector requests access to the second storage region (41b) of the memory (i.e., the memory 41 as shown in Fig. 4).

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Although Anderson >946 not specifically specifying the particular region of memory (DRAM 346/RAM 532) for storing the image data from the photoelectric converter (224), the memory such that DRAM/RAM as used in the system of Anderson >946 is extremely well-known to pertain a different storage region for separately storing the image data and the image related data such as the Header data, ID data and the Management data. This is further evidenced by Anderson >946, because Anderson >964 stated at col. 5, lines 35 that the memory, e.g., RAM disk 532, is organized in a Asectored≡ format (i.e., noted the Asectored≡ format of ROM as shown in Fig. 5) similar to that of conventional hard disk drives.

In view of this, the Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the well-known and standardized file system by storing the image data in the second region of the memory (i.e., the image storing regions of DRAM 346/RAM 532) so as to permit external host computer system (i.e., the external device as claimed), via I/O 348, to readily recognize and access the data stored on memory (i.e., DRAM 346/RAM 532 of Anderson >946) when external host computer system (i.e., the external device) connected to the connector (i.e., the element 348 of Anderson >946) requests access to the second storage region of the memory (i.e., The image storage region of DRAM 346/RAM 532 of Anderson >946).


Conclusion

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aung S. Moe whose telephone number is 571-272-7314. The examiner can normally be reached on Mon-Fri (9-5).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on 571-272-7308. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Aung S. Moe
Primary Examiner
Art Unit 2612

A. Moe
April 19, 2005